CLAIMS

We claim:

1. An interconnect structure comprising:

a substrate;

a plated through hole positioned within the substrate;

a redistribution layer on a first and a second surface of the substrate; and

a via within the redistribution layer, selectively positioned ~~over~~ and electrically connecting the plated through hole.

2. The interconnect structure of claim 1, wherein the substrate comprises:

a ground plane;

a first dielectric layer over a first and a second side of the ground plane;

a first pair of first signal planes, one over each first dielectric layer;

a second dielectric layer substantially over each first signal plane;

a first pair of first power planes, one over each second dielectric layer;

a third dielectric layer substantially over each first power plane;

a second pair of second signal planes, one over each third dielectric layer;

a fourth dielectric layer substantially over each second signal plane; and

a second pair of second power planes, one over each fourth dielectric layer.

3. The interconnect structure of claim 2, wherein the ground plane comprises copper-Invar-copper.

4. The interconnect structure of claim 2, wherein the first and second signal planes are layers of controlled impedance circuitry.

5. The interconnect structure of claim 2, wherein the first, second, third and fourth dielectric layers comprise a polytetrafluroethylene material filled with silicon particles.

6. The interconnect structure of claim 1, wherein the redistribution layer comprises a fatigue resistant dielectric material.

7. The interconnect structure of claim 1, wherein the via includes a portion of a chip connector.

8. The interconnect structure of claim 7, wherein the chip connector is selected from the group consisting of: controlled collapse chip connectors, ball grid array connectors and reflow solder attach connectors.

9. The interconnect structure of claim 1, wherein the via is offset from the center of the plated through hole.

10. The interconnect structure of claim 1, wherein the plated through hole includes copper plating.

11. The interconnect structure of claim 1, wherein the plated through hole further includes a fill material.

12. The interconnect structure of claim 11, wherein the fill material is a reinforcing material.

13. The interconnect structure of claim 12, wherein the reinforcing material comprises an electrically conductive material.

14. The interconnection structure of claim 1, further including a buried plated through hole within the substrate.

15. A method of forming a semiconductor chip carrier, comprising the steps of:

providing a substrate, having a plated through hole therein;

depositing a redistribution layer on a first and a second surface of the substrate; and

forming a via within the redistribution layer, selectively positioned over and electrically contacting the plated through hole.

16. The method of claim 15, further including the step of:

forming a chip connection pad in the via.

17. The method of claim 15, wherein the step of providing a substrate, having a plated through hole therein includes the steps of:

drilling a hole through the substrate;

cleaning the hole; and

forming a conductive layer on an interior surface of the hole.

18. The method of claim 15, further comprising the step of:

filling the plated through hole with a reinforcing material.

19. The method of claim 18, wherein the reinforcing material comprises an electrically conductive material.

20. The method of claim 15, wherein the step of depositing the redistribution layer is performed using a lamination process.

21. The method of claim 15, wherein the step of providing a substrate, having a plated through hole therein further includes the steps of:

providing a ground plane;

forming a first pair of signal planes within the substrate;

forming a first pair of power cores within the substrate;

forming a second pair of signal planes within the substrate; and

forming a second pair of power cores within the substrate.

22. The method of claim 21, wherein the first and second pair of signal planes are controlled impedance circuitry.

23. The method of claim 21, wherein the second pair of power cores are directly underneath and electrically connected to portions of the redistribution layer.

24. The method of claim 23, wherein the second pair of power cores further includes a top surface metallurgy (TSM) and a bottom surface metallurgy (BSM).

25. The method of claim 15, wherein the redistribution layer comprises a fatigue resistant dielectric material.

26. The method of claim 15, further comprising the step of:

providing a buried plated through hole in the substrate.

27. A semiconductor chip carrier comprising:

a substrate having a plated through hole therein; and

a flexible fatigue resistant redistribution layer on a first and second surface of the substrate. or directly covering PWV cores

28. The semiconductor chip carrier of claim 27, further comprising:

a via within the fatigue resistant redistribution layer, positioned over and physically contacting the plated through hole.

29. The semiconductor chip carrier of claim 27, further including a buried plated through hole within the substrate.